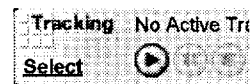


DELPHION**RESEARCH****PRODUCTS****INSIDE DELPHION****Log Out** **Work Files** **Saved Searches**

My Account

Search: Quick/Number Boolean Advanced Derwent

The Delphion Integrated View

Get Now: ☒ PDF | [File History](#) | [Other choices](#)

Tools: Add to Work File: Create new Work F

View: INPADOC | Jump to: Top

Go to: Derwent

Email ti

Title: **JP06302963A2: MULTILAYER CIRCUIT BOARD AND ITS MANUFACTURE**

Derwent Title: Multilayer circuit substrate fabrication - using through hole plated substrate to achieve interlayer access with alternate insulating layers [Derwent Record]

Country: **JP** Japan

Kind: **A**

Inventor: **SHIMAMOTO TOSHIJI;**

Assignee: **TOKUYAMA SODA CO LTD**
[News](#), [Profiles](#), [Stocks](#) and [More about this company](#)

Published /
Filed: **1994-10-28** / 1993-04-13

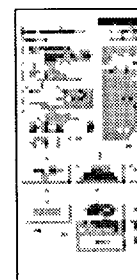
Application
Number: **JP1993000086499**

IPC Code: Advanced: [H05K 3/00](#); [H05K 3/42](#); [H05K 3/46](#);
 Core: more...
 IPC-7: [H05K 1/11](#); [H05K 3/40](#); [H05K 3/46](#);

Priority
Number: 1993-04-13 **JP1993000086499**

Abstract: **PURPOSE:** To form a high-density wiring pattern with highly reliable through holes by forming a first wiring pattern on the smoothed surface of a conductive layer containing the through holes.

CONSTITUTION: The circuit board uses a copper-clad glass epoxy laminated board as an insulating substrate 2 having conductive layers 1 on both surfaces and, after forming through holes 3 with a drill, plated-copper layers 4 are formed on the internal surfaces of the holes 3 and entire surface of the substrate 2 by electroplating after performing electroless plating. The layers 4 are formed by the electroless plating and electroplating after the holes 3 with the layers 4 are filled with a thermosetting solder resist as a curable insulating resin 5 and the resin 5 is hardened and the surface of the conductive layers 4 containing the curable insulating




resin is polished by successively using a No.320 and No.600 buffs. In this multilayer circuit board, therefore, a second wiring pattern 8 can be formed on a first wiring pattern 6 with an insulating layer 7 in between at a high wiring density and with high reliability.

COPYRIGHT: (C)1994,JPO

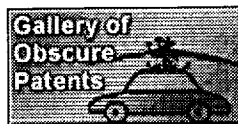
Family: None

Forward
References:

Go to Result Set: Forward references (1)

PDF	Patent	Pub.Date	Inventor	Assignee	Title
	US6426011	2002-07-30	Kato; Takashi	International Business Machines Corporation	Method making circuit b

Other
Abstract Info:



Nominate this for the Gallery...

Copyright © 1997-2006 The Thoms

[Subscriptions](#) | [Web Seminars](#) | [Privacy](#) | [Terms & Conditions](#) | [Site Map](#) | [Con](#)

Abstract

PURPOSE: To form a high-density wiring pattern with highly reliable through holes by forming a first wiring pattern on the smoothed surface of a conductive layer containing the through holes.

CONSTITUTION: The circuit board uses a copper-clad glass epoxy laminated board as an insulating substrate 2 having conductive layers 1 on both surfaces and, after forming through holes 3 with a drill, plated-copper layers 4 are formed on the internal surfaces of the holes 3 and entire surface of the substrate 2 by electroplating after performing electroless plating. The layers 4 are formed by the electroless plating and electroplating after the holes 3 with the layers 4 are filled with a thermosetting solder resist as a curable insulating resin 5 and the resin 5 is hardened and the surface of the conductive layers 4 containing the curable insulating resin is polished by successively using a No.320 and No.600 buffs. In this multilayer circuit board, therefore, a second wiring pattern 8 can be formed on a first wiring pattern 6 with an insulating layer 7 in between at a high wiring density and with high reliability.